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Machine Learning based Power Converter Large Signal Simulation for Energy Harvesting Applications

G. Vergos, V. Gogolou, C. Panagiotopoulou, A. Avgoustidis, T. Noulis, K. Siozios, S. Siskos
Physics Department, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece
{gvergos, chpanagi, anavgous, tnoul, ksiop, siskos}@auth.gr

***Abstract*—Machine learning (ML) algorithms are utilized for the implementation of a ML python-based model of dynamic behavior of Power DC – DC converters, for energy harvesting applications. This subfield of artificial intelligence, defined as the capability of a machine to imitate intelligent human behavior, is used to perform complex tasks in a way that is similar to how a designer is implementing nonlinear switching circuits, like a power DC-DC converter. The dynamic behavior of this nonlinear vehicle is simulated with ML, and in particular all the related dynamic characteristics, obtained with large signal time domain simulation, such as dynamic voltage drop – electro migration and time domain operation, are now captured rapidly with a ML approach. The related results are benchmarked versus transistor level simulations, depicting superior accuracy in minimum simulation time.**

***Index Terms*—machine learning, DC – DC converter, nonlinear circuits, switching circuits, large signal simulation**

I. Introduction

DC – DC power converter topologies are widely used in various industrial fields such as uninterruptible power supply (UPS), electric or hybrid vehicles, medium-voltage DC (MVDC) and high-voltage DC (HVDC) power systems [1]. Buck, boost, or buck-boost schemes are utilized in order to provide regulated power supply to the converter's output, independent of input energy and load variations. With the emergence of the energy harvesting concept, DC – DC conversion schemes are utilized, in order to provide matching between the ambient source and the load impedance [2]. Typically, boost DC – DC converter configurations are selected, as they offer a stepped-up output voltage, suitable for the supply of off-the-shelf components (i.e., microcontroller units, sensor modules, transmitter/receivers) [3]–[5].

As the technology progresses and the applications become more demanding, the design effort is focused on silicon integrated small-sized, low cost and energy efficient power conversion solutions [6]. However, the on-chip integration of switching circuits experiences significant design challenges. To enable high operation performance, many simulation sets must be executed, in order to determine the ideal components' characteristics of the DC – DC converter (i.e., power switches sizing, inductor and capacitor values, switching frequency). However, the DC – DC converter, which acts as a strongly nonlinear circuit due to the power switches, imposes severe restrictions regarding the simulations of time domain signals [7]. The main issue is the long simulation times due to large netlist sizes, as well as the high number of iterations needed for the design optimization. In many cases, the time-domain analysis is prematurely terminated, as the required simulation time step is ultra-small, and the total simulation time is not practical [8]. This phenomenon can lead to degraded final performance, lower power conversion efficiency and incomplete power integrity analysis, which affect the reliability of the final system.

To this end, various works have been proposed, aiming for accurate modeling of the DC – DC converter dynamic behavior and related characteristics, such as dynamic voltage drop – electro migration and time large signal - time domain analysis. These methods, mainly focused on the modeling of the power switches, are based on equivalent spice circuits or additional tools and custom co-simulation approaches (i.e., TCAD, MATLAB/Simulink) which increase the complexity of the design flow and do not contribute to the minimization of the simulation time needed [9]–[12].

Data-driven modeling for power electronics applications is an attractive solution. Machine learning based algorithms present the advantages of black box approaches (network theory analysis) combined with low-complexity low-cost software implementation, enabling design cycle speedup with high-accuracy results [7], [13]. Machine learning enables modeling of the DC – DC converter transient state characteristics by simply analyzing the given input and output data. Furthermore, the training process, which is the time-consuming part of the ML method, is executed only once. Thus, design cycle speedup is achieved.

In this work, a ML python-based model of dynamic behavior of power DC – DC converters is proposed,

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aiming to minimize simulation iterations, accurate simulation results and design cycle speedup. The behavior of this non-linear vehicle is simulated with ML, and in particular all the related dynamic characteristics obtained with large signal time domain simulation are captured rapidly with a ML approach. The related results are benchmarked versus transistor level simulations, depicting superior accuracy in minimum simulation time.

The rest of the paper is summarized as follows: Section II introduces the architecture of the employed dataset that is used as a baseline for evaluating the proposed solution. Section III describes the proposed simulation framework and highlight the customization phase of the employed machine learning solution. Benchmark results that evaluate the efficiency of the proposed solution as compared to the ground-truth simulation data (retrieved from commercial simulation tools) are summarized at Section IV. Finally, Section V concludes the paper.

II. Machine Learning Algorithm Input Data Selection

Fig. 1 depicts the schematic of the DC – DC synchronous boost converter topology. The circuit consists of an inductor (L), a low-side (S2) and a high-side (S1) power switch and the input/output capacitors (Cin, Cout). The captured energy is stored in the inductor component, and it is released to the output capacitor, providing a stepped-up voltage [14].

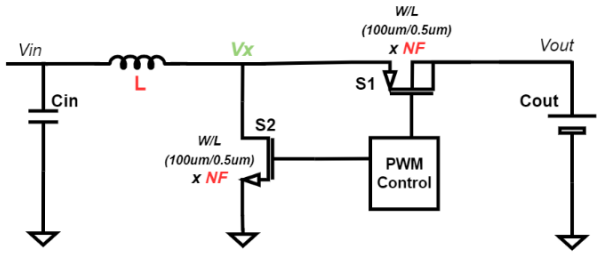
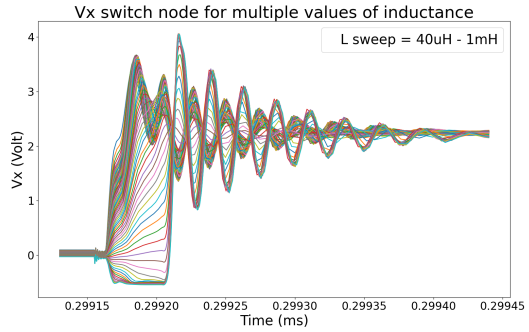


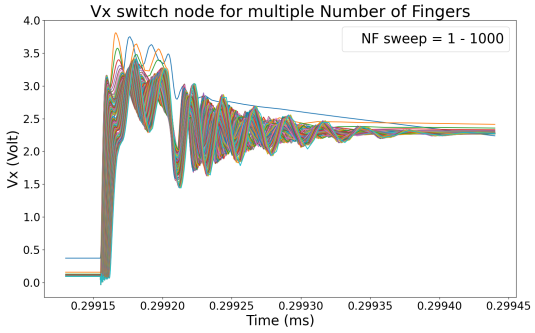
Fig. 1. Boost DC -DC converter schematic

The power MOSFETs of the DC – DC converter, experience voltage overshoots due to significant ringing on the switch node (Vx), where the two MOSFETs and inductor are tied together. If the amplitude of the ringing exceeds the absolute maximum voltage ratings of the CMOS process, it can be destructive to the chip. Furthermore, phenomena such as electromagnetic interference (EMI) can affect the performance of other circuits within close range [15].

To this end, the transient voltage signal at the switch node Vx is selected as the main performance metric for the proposed large signal simulation methodology. The DC - DC boost converter is simulated in XFAB CMOS



(a) Vx switch node transient signals for various inductance values



(b) Vx switch node transient signals for various Number of Fingers.

Fig. 2. Vx switch node time domain signal versus multiple values of inductance L and Number of Fingers NF

0.18 μm Process Design Kit. To provide realistic results, the simulation testbench includes the bond wires' parasitic inductances, represented with 2nH/mm inductors. The Vx transient signals are captured for a 300 μsec time window with 200 psec time step, depicting S1 switch turn ON. Two datasets, with two different variables are provided as input data to the machine learning algorithm. The first set provides transient signals for varying inductances (L) from 40 uH to 1 mH (Fig. 2a). The second dataset provides transient signals for varying MOSFETs size, with single finger ratio 100 μm/ 0.5 μm (Fig. 2b). The number of fingers multiplicity factor (NF) is swept from 1 to 1000. The datasets are extracted in .csv format files in order to be compatible with the ML algorithm input specifications. Each dataset simulation (generation) time is around 25 hours. One ML model was trained for each waveform in the time-domain data and one model for the highest peak values as well as second, third highest etc, for the different values of L and NF. These specific variables are selected in order to validate the ML method accuracy. Depending on the design though, the analysis can be adjusted for the extra DC – DC converter parameters, such as switching frequency, dead-time duration, input and/or output capacitance values.

III. Employed Neural Network Modeling Methodology

A. Architecture Description

The Neural Network (NN) takes one input and produces one output and It consists of two hidden layers of length 1024 as shown on Fig. 3. The dataset consists of waveforms, therefore the activation function of the first hidden layer is Tanh [16], [17]. Tanh is a non-linear sigmoid function with values ranging from -1 to 1. This means that big negative values are going to produce an output close to -1, and values close to 0 are going to produce values close to 0. The NN performs well with just the first hidden layer but adding a second one with a ReLU activation function increases the performance a lot. ReLU is a function which returns 0 for negative values and the same value for positive values. Finally, the NN uses the Adam optimizer which is fast and works well with most activation functions [18].

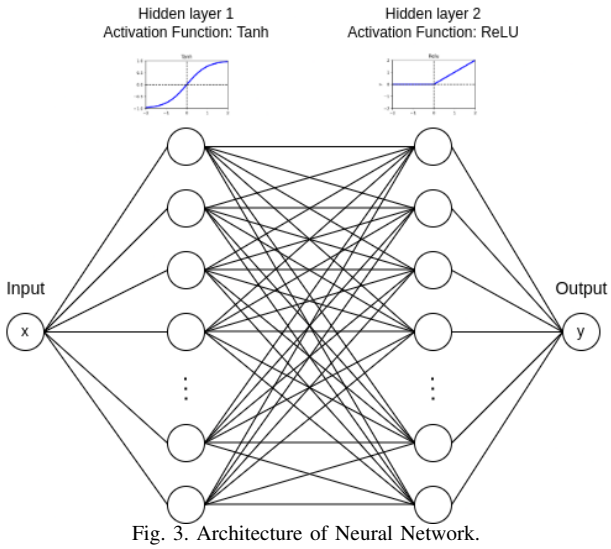


Fig. 3. Architecture of Neural Network.

B. Customization and Metrics

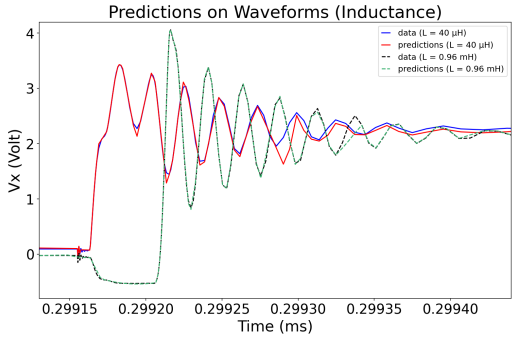
The dataset is split into training set and test set. The first is used to train the model while the other is used for validation. During the training process, the NN model calculates the loss on the test set from the forward pass and then backpropagates using the optimizer to tweak the weights and biases of all the neurons. Hence the performance of the model increases when this repetitive process increases. Each iteration is called an *Epoch* and more Epochs results in more training time. The loss is calculated using the Mean Squared Error loss function. The optimization during backpropagation is done with Adam optimizer. After the training process, the model's performance is evaluated using the Mean Absolute Error (MAE), Root Mean Squared Error (RMSE) and the Mean Absolute Percentage Error (MAPE) (1).

$$
\begin{aligned}
MAE &= \frac{1}{N_{test}} \sum_{n=1}^{N_{test}} |d_n - y_{o,n}| \\
RMSE &= \sqrt{\frac{1}{N_{test}} \sum_{n=1}^{N_{test}} (d_n - y_{o,n})^2} \\
MAPE &= \frac{1}{N_{test}} \sum_{n=1}^{N_{test}} |\frac{d_n - y_{o,n}}{d_n}| \times 100\%
\end{aligned}
\tag{1}
$$

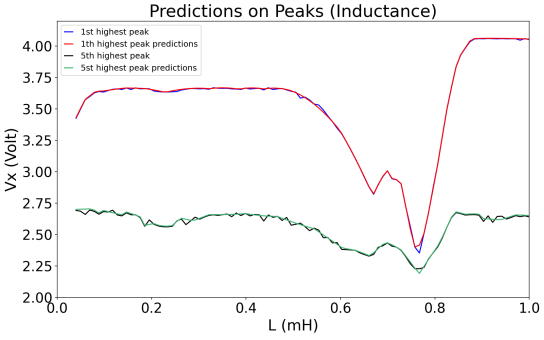
where N_{test} is the total number of testing patterns, d_n is the n-th sample value from the test dataset and $y_{o,n}$ is the n-th prediction output.

IV. Machine Learning Modeling Benchmarking

Fig 4a shows the voltage output in the time domain from SPECTRE virtuoso based simulation, for different values of inductance 40 μH and 0.96 mH, which are the edges of the L value in the design space. The red line is the model's prediction. Similarly Fig. 4b shows the voltage output peak value of the first and fifth highest peaks, with respect to the different values of inductance.

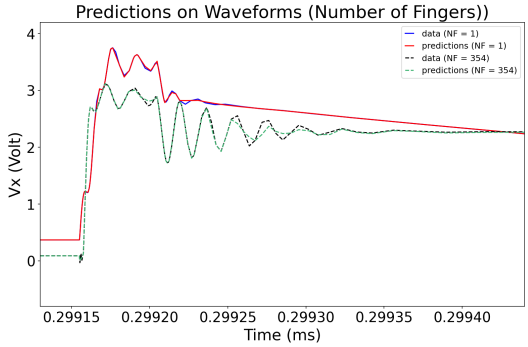


(a) Vx switch node time domain voltage and model prediction for inductance values of 40 µH and 0.96 mH

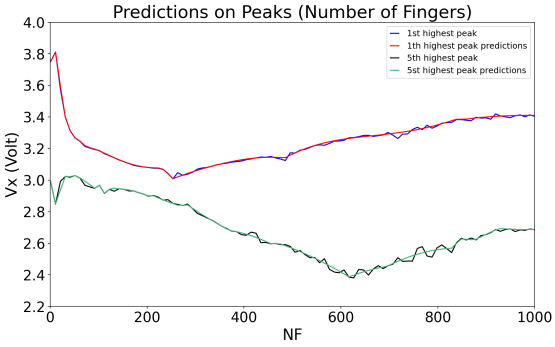


(b) Vx switch node peak value of the first and fifth highest peaks, with respect to different values of inductance.

Fig. 4. Converter ML Model vs Standard simulation



(a) Vx switch node time domain voltage and model prediction for 1 and 354 fingers



(b) Vx switch node peak value of the first and fifth highest peaks, with respect to different number of fingers.

Fig. 5. Converter ML Model vs Standard simulation

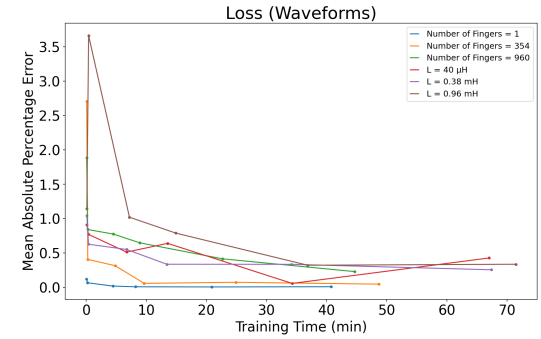
Extra plots were generated with the ML based modeling approach for different numbers of fingers in the Converter MOSFETs. This analysis was performed to examine the ML model accuracy in terms of the MOSFETs sizing . In Fig. 5 the ML model is benchmarked versus standard SPECTRE based simulations. The accuracy is superior since the model accurately captures the referenced waveforms as well as the exact peak values.

Table I displays the results from the waveforms and peaks training for different values of inductance L and number of fingers NF. The Training Time (TT) of the model is heavily dependent on the number of Epochs, while the Prediction Time (PT) is less than a millisecond in all cases. Finally, we present the error metrics results in order to evaluate the model's performance. The TT is in the order of minutes which is very small. The MAE, RMSE and MAPE values are really small with a MAPE average for 1000000 epochs of 0.217 for the waveforms and 0.0032 for the peaks. This means that the model can estimate with great accuracy the transition state of the circuit and therefore the large signal transient operation.

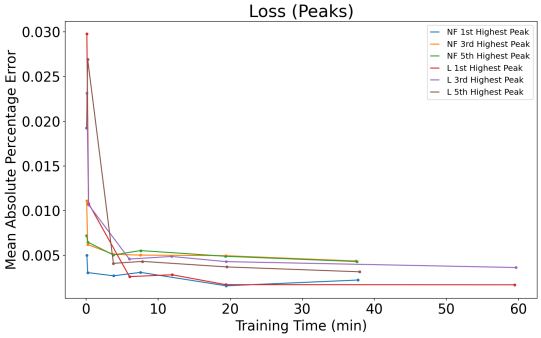
Fig. 6 shows the value of the MAPE metric when training the model for 1000, 3000, 5000, 100000, 200000, 500000 and 1000000 Epochs. The horizontal axis portrays the TT needed for the model's to train. It is clear that with more Epochs the Error minimizes while the TT increases. For 1000000 Epochs the TT ranges from 60 to 70 minutes. As it is obvious through the benchmarking of the ML model results versus to the standard transistor level simulation, the accuracy obtained is way satisfactory while the simulation time is minimal. This is valid, either the ML estimates the impact of the transistor sizing through the number of fingers sweep, or the inductance value. As clearly depicted in Fig.5, the higher the training time, the better the accuracy obtained.

Table I. Results

Inductance												
	Waveforms						Peaks					
Epochs	L (mH)	TT (min)	PT (ms)	RMSE	MAE	MAPE	Peak	TT (min)	PT (ms)	RMSE	MAE	MAPE
200000	0.004	13.54	0.84	0.0425	0.0299	0.64	1st	11.93	0.46	0.0128	0.0098	0.0028
	0.38	13.4	0.86	0.0455	0.027	0.3364	3rd	11.83	0.78	0.0178	0.0138	0.0048
	1	14.9	0.87	0.1019	0.0688	0.789	5th	7.8	0.44	0.0162	0.0112	0.0043
1000000	0.004	67	0.57	0.0328	0.0192	0.427	1st	59.45	0.51	0.0087	0.0058	0.0017
	0.38	67.42	0.58	0.0387	0.0286	0.2558	3rd	89.64	0.5	0.014	0.0104	0.0036
	1	71.47	0.44	0.431	0.0231	0.3363	5th	37.95	0.5	0.0141	0.0081	0.0031
Number of Fingers												
	Waveforms						Peaks					
Epochs	NF	TT (min)	PT (ms)	RMSE	MAE	MAPE	Peak	TT (min)	PT (ms)	RMSE	MAE	MAPE
200000	1	8.19	0.76	0.0327	0.0187	0.00945	1st	7.55	0.43	0.0285	0.0107	0.0031
	354	9.64	0.52	0.0896	0.0406	0.0583	3rd	7.53	0.43	0.0297	0.0145	0.005
	960	8.89	0.77	0.0437	0.0254	0.6482	5th	7.56	0.43	0.0342	0.015	0.0055
1000000	1	40.75	0.55	0.016	0.0112	0.00851	1st	37.73	0.47	0.0262	0.0077	0.0023
	354	48.66	0.56	0.0176	0.0083	0.0469	3rd	37.38	0.51	0.0294	0.0143	0.0043
	960	44.64	0.55	0.0558	0.0478	0.2295	5th	37.6	0.5	0.0321	0.0132	0.0043



(a) Waveforms



(b) Peaks

Fig. 6. MAPE values for different amount of Training Time (TT)

V. Conclusions

An innovative Machine Learning based modeling and simulation approach was developed, accurate to estimate efficiently the large signal - time domain operation of a non linear circuit vehicle, which in this case is CMOS a boost converter. Specific design parameters were used as input data, such as the inductance value of the converter and the sizing of the MOSFET devices (and therefore the impact of the impedances of the devices) to train the ML model. The ML provides high accurate results as long as the training time is adequate enough. The time domain response is ML wise, simulated accurately and the peaks of the converter output signal bounce behavior are efficiently captured. The above methodology enables high design cycle speed up since the large number of standard SPECTRE or SPICE time domain parametric simulations are now avoided.

Acknowledgment

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